**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:**

1. (Currently amended) An active matrix backplane used within a display, comprising:

a plurality of pixels; [[and]]

a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of a plurality of pixel transistors; and/or

a plurality of row transistors, wherein at least two row transistors within said plurality of row transistors turns a corresponding pixel transistor on and off; and

a plurality of pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels, wherein each pixel transistor within said plurality of pixel transistors, each column transistor within said plurality of column transistors and each row transistor within said plurality of row transistors [[is a]] are nanowire ~~transistor~~ transistors comprising a plurality of nanowires extending between a first source electrode and a first drain electrode of the transistor, wherein the nanowires include a core made of a first material and a shell layer made of a second material disposed about said core, wherein said first material is compositionally different from said second material, and wherein each nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a pixel at a desired rate.

2-4. (Cancelled).

5. (Currently amended) The active matrix backplane of claim [[4]] 1, wherein each column nanowire transistor comprises at least ~~two~~ one hundred nanowires extending at least between a source and a drain electrode.

6-8. (Cancelled).

9. (Currently amended) The active matrix backplane of claim [[7]] 1, wherein each row nanowire transistor comprises at least one hundred nanowires extending at least between a source and a drain electrode. ~~an average number of nanowires sufficient to at least charge and discharge a respective pixel at a desired rate~~.

10. (Original) The active matrix backplane of claim 1, further comprising nanowire edge electronics.

11. (Original) The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire buffers.

12. (Original) The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire shift registers.

13. (Original) The active matrix backplane of claim 10, wherein nanowire edge electronics include nanowire level shifters.

14. (Original) The active matrix backplane of claim 1, wherein the display is a liquid crystal display.

15. (Original) The active matrix backplane of claim 1, wherein the display is an organic light emitting display (OLED).

16. (Original) The active matrix backplane of claim 15, wherein said OLED includes nanocrystals.

17. (Original) The active matrix backplane of claim 1, wherein the display is an electrophoretic display.

18. (Original) The active matrix backplane of claim 1, wherein the display is a plasma display.

19. (Original) The active matrix backplane of claim 1, wherein the display is an electrochromic display.

20. (Original) The active matrix backplane of claim 1, wherein the display is a microelectromechanical (MEMs) display.

21. (Original) The active matrix backplane of claim 1, wherein the display is a micromirror display

22. (Original) The active matrix backplane of claim 1, wherein the display is a field emission display.

23. (Original) The active matrix backplane of claim 22, wherein the display is a nanotube field emission display.

24. (Original) The active matrix backplane of claim 1, wherein the display is rigid.

25. (Original) The active matrix backplane of claim 1, wherein the display is flexible.

26. (Original) The active matrix backplane of claim 1, wherein the display is non-planar.

27. (Currently amended) A liquid crystal display having a base substrate comprising:

(a) a plurality of pixels;

(b) a plurality of pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels;

(c) a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of said plurality of pixel transistors; and

(d) a plurality of row transistors, wherein at least two row transistors within said plurality of row transistors ~~turns~~ turn a corresponding pixel transistor on and off, wherein at least one of: i) said plurality of pixel transistors, ii) said plurality of column transistors, and iii) said plurality of row transistors are nanowire transistors comprising a plurality of nanowires extending between a first source electrode and a first drain electrode of the nanowire transistor, wherein the nanowires include a core made of a first material and a shell layer made of a second material disposed about said core, wherein said first material is compositionally different from said second material, and wherein each nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a pixel at a desired rate.

28. (Original) The liquid crystal display of claim 27, further comprising nanowire edge electronics.

29. (Original) The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire buffers.

30. (Original) The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire shift registers.

31. (Original) The liquid crystal display of claim 28, wherein nanowire edge electronics include nanowire level shifters.

32. (Original) The liquid crystal display of claim 27, wherein pixel transistors within said plurality of pixel transistors, column transistors within said plurality of column transistors, and row transistors within said plurality of row transistors are nanowire transistors.

33. (Currently amended) The liquid crystal display of claim 27, wherein at least one of: i) said plurality of pixel transistors, ii) said plurality of column transistors, and iii) said plurality of row transistors are a-Si thin film transistors.

34. (Currently amended) The liquid crystal display of claim 27, wherein at least one of: i) said plurality of pixel transistors, ii) said plurality of column transistors, and iii) said plurality of row transistors are bulk Si thin film transistors.

35. (Currently amended) The liquid crystal display of claim 27, wherein at least one of: i) said plurality of pixel transistors, ii) said plurality of column transistors, and iii) said plurality of row transistors are organic semiconductors.

36. (Currently amended) The liquid crystal display of claim 27, wherein at least one of: i) said plurality of pixel transistors, ii) said plurality of column transistors, and iii) said plurality of row transistors are poly-Si thin film transistors.

37. (Original) The liquid crystal display of claim 27, wherein nanowires used to form the transistors are aligned substantially parallel.

38. (Original) The liquid crystal display of claim 27, wherein the wires are aligned one of substantially randomly and isotropically.

39. (Original) The liquid crystal display of claim 27, wherein nanowire column transistors are located between column traces.

40. (Original) The liquid crystal display of claim 27, wherein nanowire column transistors are located inline with the column traces.

41. (Original) The liquid crystal display of claim 27, wherein nanowire row transistors are located between row traces.

42. (Original) The liquid crystal display of claim 27, wherein nanowire row transistors are located inline with row traces.

43. (Cancelled).

44. (Original) The liquid crystal display of claim 27, wherein a nanowire transistor comprises at least ten nanowires connecting a source to a drain electrode of the nanowire transistor.

45. (Previously presented) The liquid crystal display of claim 27, wherein a nanowire transistor comprises at least one hundred nanowires connecting a source to a drain electrode of the nanowire transistor.

46. (Original) The liquid crystal display of claim 27, wherein the base substrate is a flexible material.

47. (Original) The liquid crystal display of claim 27, wherein the base substrate is a low temperature material with a melting temperature below 500 degrees Fahrenheit.

48. (Original) The liquid crystal display of claim 27, wherein the base substrate is a plastic.

49. (Original) The liquid crystal display of claim 27, wherein the base substrate is translucent material.

50-51. (Cancelled).

52. (Currently amended) An active matrix backplane used within a display, comprising:

a plurality of pixels;

a plurality of amorphous silicon pixel transistors, wherein a pixel transistor within said plurality of pixel transistors controls a corresponding pixel within said plurality of pixels; and

a plurality of column transistors, wherein a column transistor within said plurality of column transistors applies a voltage across a subset of said plurality of pixel transistors, and wherein each column transistor within said plurality of pixel transistors is a nanowire transistor comprising a plurality of nanowires extending between a first source contact and a first drain contact of the transistor, wherein the nanowires include a core made of a first material and a shell layer made of a second material disposed about said core, wherein said first material is compositionally different from said second material, and wherein each nanowire transistor comprises an average number of nanowires sufficient to at least charge and discharge a pixel at a desired rate.

53. (Cancelled)

54. (Previously presented) The active matrix backplane of claim 1, wherein the first material includes silicon and the second material includes $SiO_2$.

55. (Previously presented) The active matrix display of claim 1, further comprising a gate contact disposed about said shell layer.

56. (Previously presented) The liquid crystal display of claim 27, wherein the first material includes silicon and the second material includes $SiO_2$.

57. (Cancelled).

58. (New) The active matrix backplane of claim 52, wherein each nanowire transistor comprises at least one hundred nanowires extending at least between a source and a drain electrode.